REMARKS

Claims 1-42 appear in this application for the Examiner's review and consideration. The allowance of claims 1-37 is noted with appreciation. Claims 38-41 are now re-written in independent form. Claim 42 has been amended to further define the invention but new matter has been introduced.

In view of the above amendments and the following remarks, the applicant respectfully requests favorable reconsideration and allowance of the application.

The sections set forth below are presented in the same order as that of the Action for ease of reference.

The Information Disclosure Statement

The Information Disclosure Statement filed on January 26, 2004 was objected to because one of the references, "Swamy et al.", purportedly had no date. A review of the initialed Form PTO-1449 attached to the present Action reveals that a copy of Swamy et al. was filed with a date (i.e., 1995) and that the reference was, in fact, considered by the Examiner. The applicant believes that the Examiner meant to cite Guerrier et al., "A Generic Architecture for On-Chip Packet-Switched Interconnections" as the reference requiring a date. Thus, enclosed herewith is a "Third Supplemental Information Disclosure Statement" again listing the Guerrier et al. reference and supplying the date as provided to us by the inventor.

The applicant believes that no fee is due for this submission as the reference was supplied to the Office before a first Action on the merits, but if a fee is due please charge deposit account no. 50-1814. The applicant also respectfully requests that the Guerrier et al. reference be considered and made of record in the application.

The Drawings

The figures were objected to for being unclear. Thus, submitted herewith are the formal drawings for this application. In view of this submission, the applicant requests withdrawal of the objection to the drawings.

Informality Objections

Claims 39, 40 and 41 were objected to for being of improper dependent form. In addition, claim 42 was objected to because the word "architective" is misspelled.

In response, claims 38-41 have now been re-written in independent form while the misspelling in claim 42 has been corrected. No new matter has been added. Included

herewith is a fee sheet as this amendment adds three (3) independent claims in excess of those already paid for. In view of these changes, withdrawal of the objections to claims 38-42 is requested.

The 35 U.S.C. 102(b) Rejections

Claims 38-40 and 42 were rejected as being anticipated by Agrawal et al, U.S. Patent 6,191,612.

Agrawal pertains to Field Programmable Gate Array (FPGA) devices that include a plurality of input/output blocks ("IOBs") and variable grain blocks ("VGBs"). The patent is particularly concerned with an inter-connect network for providing flexible routing of control signals from the VGBs to the IOBs (see Fig. 1 and col. 6, line 31 to col. 7, line 2 of Agrawal).

In contrast, pending independent claim 38 recites an integrated circuit having a plurality of logic areas and an actively switchable network selectively connecting one logic area with another logic area. An actively switchable network in the context of the present invention is a network that includes communication resources that are actively shared between many logic areas, and where logical connections switch rapidly according to the communication needs at any particular time of the logic areas sharing the communication resource. Not included in this definition are networks where a permanent or semi-permanent connection is made to connect or transmit individual signals or single data bits between specific areas of logic (see application, page 2, line 33 to page 3, line 6). Conversely, the integrated circuit disclosed by Agrawal includes at least five metal layers for forming inter-connect lines, and direct lines and long lines are preferably implemented entirely by the metal layers to provide for low-resistance pathways (see col. 6, lines 36-41). Thus, Agrawal's integrated circuit contains a network that includes permanent or semi-permanent connections between specific logic areas. The integrated circuit disclosed by Agrawal therefore fails to teach or suggest the actively switchable network as recited by claim 38. Consequently, claim 38 is not anticipated.

As noted above, claims 38 to 40 are now re-written in independent form to expressly include all features of claim 1. Since claim 1 has been allowed, claims 38 to 40 should be allowable for at least the same reasons.

Claim 42 recites an integrated circuit having an architecture comprising arrays of logic gates or logic blocks, and an on-chip packet-switching network. Claim 42 has been amended to recite that a packet comprises a group of signals including a header that contains a location of a destination functional block. In contrast, Agrawal teaches an integrated circuit

(see Fig. 1) that includes four CBBs that can store a corresponding 4 bits of data so as to define a nibble of data for output onto adjacent inter-connect lines. Each VGB contains four CBBs which can acquire and process a nibble's worth of data (see Agrawal, col. 7, lines 10-34). Thus, Agrawal fails to teach or suggest a packet switching structure as now recited in claim 42, and thus claim 42 is not anticipated and should be allowable.

In view of the above amendments and remarks, the applicant requests withdrawal of the 35 U.S.C. 102(b) rejections of claims 38-40 and 42.

The prior art made of record and not relied upon has not been discussed herein as none of those references has been applied to any of the claims.

Conclusion

In view of the above, all rejections have been overcome so that the entire application is believed to be in condition for allowance, early notice of which would be appreciated. Should any issues remain, a personal or telephonic interview is respectfully requested to discuss the same in order to expedite the allowance of all the claims in this application.

Respectfully submitted,

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